

# EI E 481: Fund. Low Power Dig. VLSI Design

Techniques to constrain designs, run static timing analysis, evaluate datapath logic, run physical synthesis, optimize for low-power structures, analyze DFT (design for test-ability) constraints, and interface with other tools. Exploration and implementation of several low-power techniques to reduce both dynamic and leakage power during synthesis, including multiple supply voltage (MSV) design, power shutoff (PSO) synthesis and dynamic voltage frequency scaling (DVFS) synthesis, low-power flow using CPF and IEEE 1801 and troubleshoot a low-power design, and formal verification of power constraints and ensure the functionality of a low-power design.

#### 3 Credits Prerequisites

<u>El E 385: Advanced Digital Systems</u> \$target.descriptions.MinimumGrade\$

• Pre-Requisite: 24 Earned Hours

# Instruction Type(s)

Lecture: Lecture for El E 481

### **Subject Areas**

Computer Hardware Engineering

## **Related Areas**

• Computer Engineering, General

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